CICS TS V4.R2
User's Experience From a Software Developer's Point of View
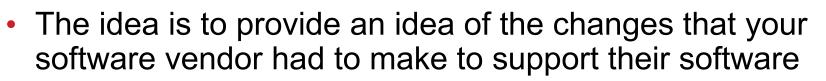
Eugene S Hudders
C\TREK Corporation
Session 9324
August 8, 2011

Agenda

- Why?
- Documentation Changes
- New (E) DSA
- Control Block Changes
- Closing

Why?

- The idea is to provide an idea of the changes that your software vendor had to make to support their software
- To alert those users that may have in-house routines that access control blocks the changes that have occurred
- To provide information to people that read control blocks found in dumps of the changes that have been made

Documentation Changes

- The most important documentation change is the elimination of
  - Supplementary Data Areas
  - Optional Source Feature
- During the Beta program in which vendors and clients participated, there were no significant issues raised regarding the removal of these two items
- If you have a specific requirement, please be sure to see Mr. Ian J Mitchell, CICS Portfolio Architect, IBM Hursley who is here at SHARE

New DSA

- There is one active (E) DSA in the release
- The new EDSA is above the line and it is called "Extended Trusted Dynamic Storage Area" or ETDSA
    - Contains the anchor blocks, control blocks and tables of
        - Anchor Blocks
            - *User Domain (US)*
            - *Security Domain (XS)*
        - Some of the Domain Sub-pools
            - *UGENERAL*
            - *USUDB*
            - *USXDPOOL*
            - *XSGENRAL*
            - *XSXMPOOL*
            - *USRTMQUEU*
- The storage area for any security-related CICS control blocks that reside in 31-bit storage
- The ETDSA is always allocated from CICS key (8)

Control Block Changes

- Major rework of the following control blocks where fields were relocated and many unused fields were deleted:
  - CSA
  - OFL
  - TCA
- Temporary Storage and Trace Domains have been changed to support 64-bit addresses for the TS Main resources and the Trace table
- Storage Manager major reorganization of the SM anchor block

Control Block Changes

- The Kernel Anchor was reworked and many pointers were expanded to 64-bit format although the control blocks associated with these pointers remained below the Bar

  - Kernel Error collects the PSW in 16 bytes and 8 byte registers

- The number of LSR pools has been increased from 8 to 255 which involved changes to the FCP SSA

Closing

- The new release had several control block updates
  - Control block changes included adding 64-bit pointers
  - TS Main and Trace Table can be placed above the Bar
- The new LSR pool structure allows for better tuning when using Threadsafe VSAM
- For more information on CICS TS V4.R2 go to the different presentations during the week